WHAT IS CLAIMED IS:

1. A SiC-MISFET comprising:

a SiC body including a body portion containing an impurity of a first conductive type;

a well region formed by introducing an impurity of a second conductive type into part of the SiC body other than the body portion;

a channel layer which is formed so as to extend over the well region and the body portion of the SiC boby in the SiC body and contains an impurity of the first conductive type;

a gate insulation film formed on the channel layer;

a gate electrode formed on the gate insulation film;

a source region which is formed in a region of the SiC body located adjacent to the channel layer so as to be in contact with the well region and contains an impurity of the first conductive type;

a drain region formed in a region of the SiC body facing to the source region with the body portion interposed therebetween; and

a partially heavily doped layer formed by implanting an impurity of the second conductive type into part of the SiC body located under the channel layer at a higher concentration than that in the well region.

2. The SiC-MISFET of claim 1, wherein a depletion layer formed due to the partial heavily doped layer reaches the gate insulation film with a voltage of 0 V applied between the gate electrode and the well region.

3. The SiC-MISFET of claim 1, wherein at least a lower surface of the partially

heavily doped layer is surrounded by the body portion, and

wherein the space between the partially heavily doped layer and the well region is shorter than a dimension of the partially heavily doped layer in the gate length direction.

4. The SiC-MISFET of claim 1, wherein the partially heavily doped layer is surrounded by the well region.

5. The SiC-MISFET of claim 4, further comprising a heavily doped contact layer which contains an impurity of the second conductive type at a higher concentration than that in the well region and is connected to the partially heavily doped layer

wherein the heavily doped contact layer is formed so as to surround the source region, and

wherein the partially heavily doped layer is formed in the same ion implantation process for forming the heavily doped contact layer.

6. The SiC-MISFET of claim 1, wherein a dimension of the partially heavily doped layer in the gate length direction is one tenth or less of a dimension of the channel layer in the gate length direction.

7. The SiC-MISFET of claim 1, wherein a dimension of the partially heavily doped layer in the depth direction is larger than a dimension of the channel layer in the depth direction.

8. The SiC-MISFET of claim 1, wherein the impurity concentration of the partially heavily doped layer is ten times or more higher than that of the well region.

9. The SiC-MISFET of claim 1, wherein the drain region is formed in a lowermost portion of the SiC body and the SiC-MISFET is a vertical type MISFET.

10. The SiC-MISFET of claim 1, wherein the drain region is formed in a surface portion of the SiC body connected to the channel layer and the SiC-MISFET is a horizontal type MISFET.

11. A method for fabricating a SiC-MISFET, comprising:

step a) of implanting an impurity of a second conductive type into other part of a body portion of a SiC body lower layer than part of the body portion containing an impurity of a first conductive type to form a well region;

step b) of implanting, before or after the step a), an impurity of the second conductive type into the body portion at a higher concentration than that in the well region to form a partially heavily doped layer;

step c) of epitaxially growing a SiC body upper layer including a channel layer containing an impurity of the first conductive type over the body portion of the SiC body, the well region and the partially heavily doped layer;

step d) of implanting an impurity of the first conductive type into part of the SiC body upper layer to form a source region;

step e) of forming a gate insulation film on the channel layer; and

step f) of forming a gate electrode on the gate insulating film.

12. The method for fabricating a SiC-MISFET of claim 11, wherein in the step b), an impurity of the second conductive type is implanted using an implantation mask having

an opening corresponding a region of the substrate in which the source region is to be formed, thereby forming the partially heavily doped layer so as to be in contact with the source region.